LeonardoSpectrum with LeonardoInsight

FPGA Synthesis

D A T A S H E E T

Proprietary ease-of-use features such as FlowTabs™ and QuickSetup enable first time FPGA synthesis.

Major product features:

- One tool, one learning curve, one set of scripts, for CPLDs, FPGAs, or ASICs
- Mix VHDL, Verilog, and EDIF to enable design reuse and instantiation of intellectual property
- Highest QoR with the speed and features you need for large designs
- HDLInventor™ creates optimized HDL code fast and facilitates company wide sharing of intellectual property
- Technology-specific F.A.S.T. Optimization ensures a fast and small design
- P&R Integrator simplifies place-and-route and delivers improved results
- Built-in partitioning speeds ASIC prototyping and verification process

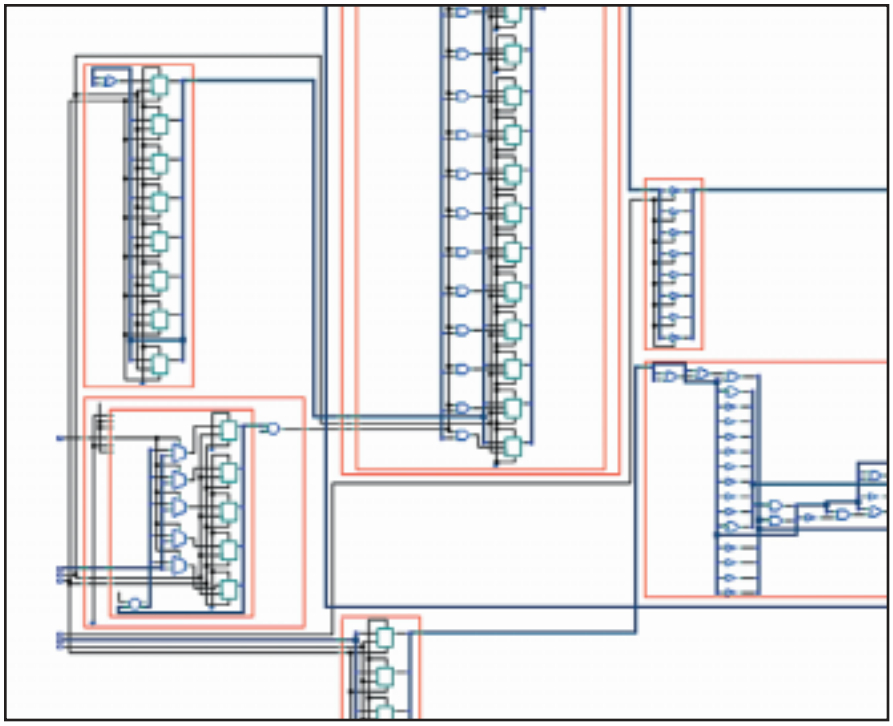
Enhance Productivity with LeonardoSpectrum

LeonardoSpectrum™ combines push-button ease of use with the powerful control and optimization features associated with workstation-based ASIC tools. LeonardoSpectrum allows you to create CPLDs, FPGAs, or ASICs in VHDL or Verilog within one synthesis environment. For design and analysis, set up is a snap, and you won't find a more flexible tool for design and analysis. A proven best-in-class solution, LeonardoSpectrum also provides synthesis horsepower for the FPGA Advantage™ flow from Mentor Graphics.

Users faced with design challenges can access advanced synthesis controls within the exclusive LeonardoSpectrum FlowTabs and PowerTabs™. In addition, the powerful debugging features and exclusive five-way cross-probing in LeonardoInsight™ accelerate your analysis of synthesis results.

Power Combined with Ease of Use

If desired, you can perform 100 percent push-button synthesis using LeonardoSpectrum. But users faced with complex designs can access advanced synthesis controls within LeonardoSpectrum's exclusive PowerTabs, which provide users with the flexibility and control to target a design to meet the speed or area requirements of that design.



LeonardoSpectrum was designed to support true hierarchical design. Its hierarchy browser allows you to access, manipulate, constrain, and interchange hierarchical blocks.

LeonardoSpectrum preserves your design hierarchy. This enables you to exploit the advantages of a hierarchical-based design approach, including both incremental design and synthesis. With .lib support and more than 200 FPGA and ASIC technologies fully supported, LeonardoSpectrum is designed to meet your needs as designs become larger, faster, and more complex.

User-Customizable Templates

There's no faster way to teach good HDL coding techniques than by example. LeonardoSpectrum allows you to insert well-architected HDL constructs into your designs using templates. You can edit built-in examples, and share your own custom-developed IP company-wide. Technology-specific templates improve resulting implementations.

Better Circuit Implementations

LeonardoSpectrum "encapsulates" FPGA vendor place-and-route (P&R) tools, allowing you to go from schematics to VHDL to back-annotation from within the same familiar GUI. LeonardoSpectrum uses the deep synthesis knowledge found in its P&R Integrator to automatically create SmartScripts™ — "intelligent" P&R scripts for vendor tools, resulting in better circuit implementations.

Supports Multiple Design Flows

LeonardoSpectrum supports your preferred design flow — flat or hierarchical, top-down, or bottom up. Whether you have IP to reuse or dozens of designers working on modules that will need to be stitched together in a bottom-up fashion, LeonardoSpectrum performs easily and automatically.

True Hierarchical Support for Incremental Synthesis

Hierarchical design enables you to perform incremental design and team design. You can modify individual modules at the RTL level, then re-synthesize and re-optimize while preserving netlist information in surrounding blocks. This significantly reduces compile times on complex, multi-block designs. An incremental approach is also supported during synthesis. Constraints can be "tightened" on sub-blocks and re-optimized to fine tune timing or area goals following place and route operations. Block-level design provides the key to efficient interaction between synthesis and place-and-route.

F.A.S.T. Optimization

LeonardoSpectrum's proprietary F.A.S.T. algorithm guarantees the highest QoR of any FPGA synthesis tool available today. Along with a dozen other design characteristics, F.A.S.T. evaluates factors such as your target technology, constraints, and number of serial elements, then automatically selects an optimization strategy to obtain the best QoR.

Scripting

Powerful scripting enables firms using LeonardoSpectrum to set up and enforce customized, company-wide design flows. Scripts can access the entire design database, providing complete data manipulation capability. Conditionals enable users to automate large, complex tasks.

Partitioning

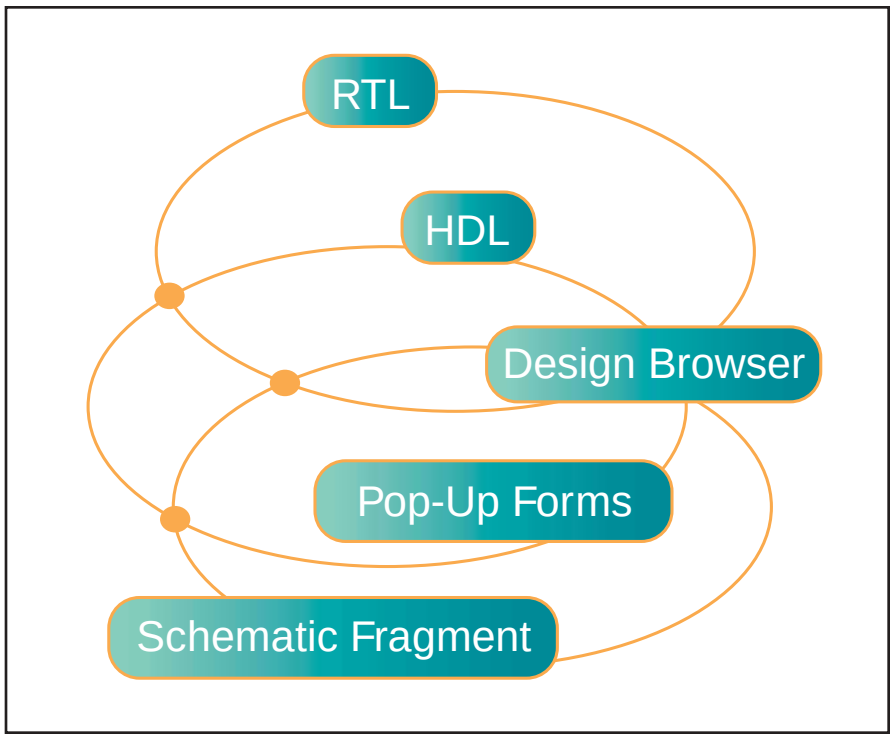
LeonardoSpectrum makes it easy to partition designs for prototyping purposes. It's often desirable to prototype a large FPGA or ASIC in multiple, smaller FPGAs. True hierarchical support makes it easy to group and ungroup design elements, which can then be targeted for single or multiple chips.

LeonardoSpectrum is the only synthesis tool that offers a truly seamless, technology-neutral environment, from FPGAs to ASICs. This allows retargeting circuits:

- When acquiring or re-using IP
- When retargeting FPGA code to an ASIC device
- When a decision is made to retarget to a new device in "mid-design"
- In order to partition and prototype ASICs using FPGAs

Independence

LeonardoSpectrum offers users platform independence, language neutrality, and target device independence. It runs on both Windows and UNIX. If you need to mix and match VHDL/Verilog IP within the same design, there's no problem. Most importantly, if code you develop for an FPGA may someday need to go into an ASIC, LeonardoSpectrum is the tool you should use. With LeonardoSpectrum you can perform automatic, error-free retargeting of existing schematics to newer field programmable devices, quickly and easily.



Five-way cross-probing lets you quickly jump between specialized debugging views.

LeonardoInsight: Debug and Analysis

No more "synthesizing in the dark" — the advanced capabilities of LeonardoInsight augment your detailed design knowledge with powerful debugging and analysis capabilities. You gain detailed insight into why different synthesis options create the results they do. With LeonardoInsight you can interactively analyze the impact of different constraint settings, coding styles and technology parameters on your overall QoR.

LeonardoInsight includes a new graphical search utility that quickly locates a variety of netlist objects through all levels of hierarchy. Once located, these objects can be cross-referenced to RTL source code inside LeonardoSpectrum, or they can be displayed in a schematic.

LeonardoInsight is designed to sit on top of the synthesis database so design directives can be applied from a graphical view with real-time updates to the database.

LeonardoInsight offers designers advanced analysis tools to track down and solve circuit bottlenecks and area budget violations, including:

Five-Way Cross-Probing

LeonardoInsight allows you to perform cross-probing among multiple design views. Each design view is optimized for a specific debugging or analysis task. This allows you to quickly obtain the information you need in order to make well-founded decisions on what to analyze next, or incrementally re-synthesize.

HDL Source Code Viewer

Understanding how synthesis results and HDL source constructs relate to one another is crucial in determining coding styles. Even small changes can improve designs by 30–40 percent or more.

Further productivity increases are available using the HDL viewer's tight integration with HDLInventor for technology-specific template selection.

RTL Block-based Schematic Viewer

You need insight into what your HDL code produces to find the best design alternatives early in the design cycle. LeonardoInsight automatically creates a block-based schematic from the RTL code before the synthesis process is even started. It utilizes familiar operator symbols. This saves time, allows you to investigate possible bottlenecks, tune hierarchy requirements and check code inferences early on in the design process.

Design Browser

The design browser in LeonardoInsight delivers crucial capabilities to reduce design time and improve overall productivity. It lets you find specific design objects, manipulate local constraints, apply synthesis directives, and manipulate or navigate the hierarchy.

The design browser shows design objects in a highly condensed form so you can find specific items quickly and easily. Preserving the design hierarchy allows rapid block, instance, port, and net selection. Bookmarks, selection filters, and cross-probing to all other views supports further analysis or manipulation.

Schematic Fragment Generator

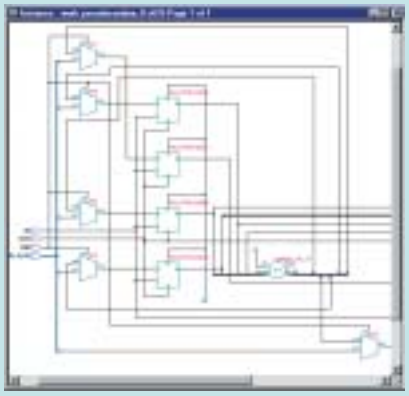
LeonardoInsight takes technology schematics to the next level of productivity. The fragment generation feature turns classic technology schematics into an effective and productive debugging view.

LeonardoInsight offers on-the-fly creation of schematics showing only critical paths, or selected paths. You can interactively extend these views in any direction — from any point along the path. Or automatically generate fan-in/out cones of logic to get a better idea of how to refine a design's timing behavior.

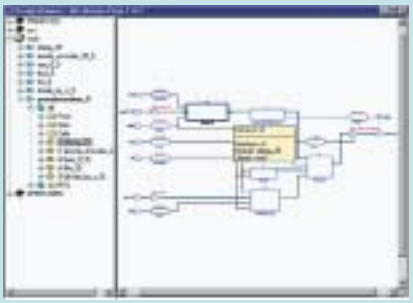
Gaining a quick and clear insight into how timing and load results are distributed in the technology implementation greatly speeds critical path analysis and your ability to effectively refine constraints for optimum area/performance tradeoffs.

Advanced Search

For large designs, LeonardoInsight's advanced search engine guides you to any port, block, signal, or gate in your design. The wild card search helps locate items of interest. With a click of the mouse, a schematic is generated with your selection highlighted.



LeonardoInsight gives you a block-based view of RTL code for considering alternatives early in the design process.



The design browser shows you a wide look at the entire design.

The Schematic Fragment Generator gives you quick insight into a design's behavior, and lets you optimize area and performance tradeoffs.

Visit our web site at www.mentor.com/synthesis for the latest product news.

Corporate Headquarters
Mentor Graphics Corporation
8005 S.W. Boeckman Road
Wilsonville, Oregon 97070 USA
Phone: 503-685-7000
North American Support Center
Phone: 800-547-4303
Fax: 800-684-1795

Silicon Valley Headquarters
Mentor Graphics Corporation
1001 Ridder Park Drive
San Jose, California 95131 USA
Phone: 408-436-1500
Fax: 408-436-1501

Europe Headquarters
Mentor Graphics Corporation
Immeuble le Pasteur
13/15, rue Jeanne Braconnier
92360 Meudon La Forêt
France
Phone: 33 (0) 1-40-94-74-74
Fax: 33 (0) 1-46-01-91-73

Pacific Rim Headquarters
Mentor Graphics (Taiwan)
Room 1603, 16F
International Trade Building
No. 333, Section 1, Keelung Road
Taipei, Taiwan, ROC
Phone: 886-2-27576020
Fax: 886-2-27576027

Japan Headquarters
Mentor Graphics Japan Co., Ltd.
Gotenyama Hills
7-35, Kita-Shinagawa 4-chome
Shinagawa-Ku, Tokyo 140
Japan
Phone: 81-3-5488-3030
Fax: 81-3-5488-3031

Printed on Recycled Paper
2-02-WCI 1020090