Precision® Hi-Rel

Siemens Digital Industries Software
Advanced FPGA Synthesis

Features and Benefits

- Broad FPGA device support
- SEU and SET mitigation across a wide spectrum of FPGA resources
- Multiple TMR configurations - LTMR/DTMR/GTMR/iSTMR
- Error detection and Error correction FSM inference for all encoding types
- Single-bit error detection across design modules
- Inference of ECC RAM modes from RTL
- Formally verifiable TMR and Safe FSM
- Configurable mitigation solution with controls from global to leaf level
- Area optimization solutions for TMR mitigation
- Intelligent synthesis enabling mitigation insertion with optimal QoR

FPGA Synthesis for Safety-Critical and High-Reliability Applications

Safety-critical and high-reliability applications pose unique challenges for FPGA designers. Safeguards must be put in place to account for single event effects that can disrupt system operation and lead to catastrophic failure. The Precision® Hi-Rel product, a Siemens EDA, a part of Siemens Digital Industries Software FPGA synthesis solution, offers unique synthesis-based capabilities for single event effects (SEE) mitigation with unmatched user control.

Advanced Safe Finite State Machines (FSM)

SEU Detect and Recovery FSM

Traditional safe finite-state machine (FSMs) optimizations available in most synthesis tools offer full single-event upset (SEU) detection and recovery for only the area-inefficient 1-hot encoding scheme. The Precision Hi-Rel product offers an enhanced form of safe FSM that offers full SEU detection and recovery for all encoding methods, including area-efficient binary and gray encoding schemes. An SEU will not cause an invalid transition or send the FSM into an unknown state.

Fault-Tolerant FSM

Some applications, however, need stronger safeguards—a safe FSM that detects an invalid transition must still go through a recovery process that typically involves an operational reset, consuming one or more clock cycles.

Because this can be prohibitive for some applications, the Precision Hi-Rel product offers a fault-tolerant FSM implementation that can absorb a SEU and continue operation without interruption. With seamless integration within the synthesis flow, and full user-control, the Precision Hi-Rel technology allows designers to implement these FSM optimizations globally, across the design or at the modular level.

Multi-Vendor Triple Modular Redundancy

Triple modular redundancy (TMR) is commonly used in high-reliability applications. Designers typically had the options of either choosing from a small number of devices with built-in TMR, developing the TMR circuitry manually, or using post-synthesis software flows. With the Precision Hi-Rel product, designers can apply TMR circuitry to a broad selection of devices from multiple vendors and avoid the time-consuming and error-prone process of manual mitigation methods. By automatically inserting TMR at the synthesis level, the Precision Hi-Rel product provides greater user control and superior quality of results when compared to post-synthesis mitigation methods.

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In Local TMR (LTMR), all designated sequential elements are tripled and followed by a majority voter, guarding against SEUs.

In Distributed TMR (DTMR), all sequential elements, combinatorial elements, and majority voters are tripled. Redundancy of combinatorial logic will guard against single-event transients (SETs)—effects that occur in combinatorial logic.

In Global TMR (GTMR) all sequential elements, combinatorial logic, majority voters, and global buffers are tripled, offering the greatest SEE immunity. When used in conjunction with a "background scrub" mechanism, DTMR and GTMR are effective for SRAM-based FPGA architectures.

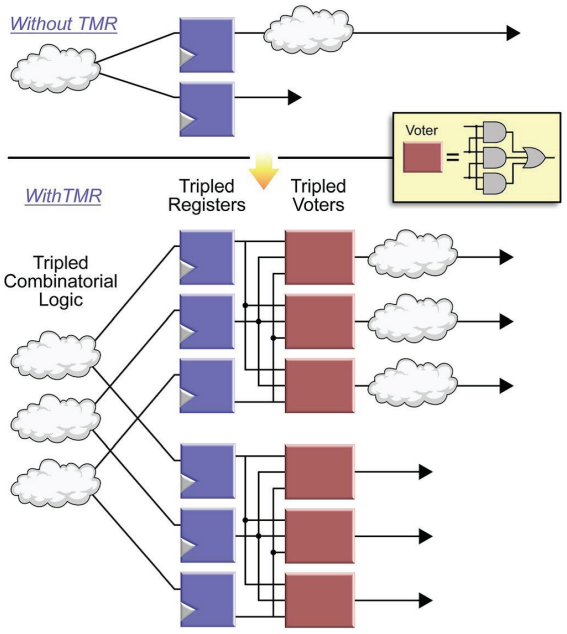
The Precision Hi-Rel's TMR technology allows for TMR implementation at the modular level and handles embedded resources such as random-access memories (RAMs), digital signal processors (DSPs), and shift register lookup tables (SRLs). Designers can seamlessly apply constraints and attributes without concern that synthesis will optimize away the TMR circuitry.

Intelligent Selective TMR (iSTMR)

In iSTMR mode, Precision Hi-Rel identifies and applies TMR on portions of the design that are structurally more susceptible to SEEs. This approach is beneficial for designs where FPGA resources are limited and a general TMR mode that results in triplication of sequential and/or combinatorial elements is not possible.

ECC RAMs

Precision Hi-Rel can infer Block RAMs with ECC mode from HDL for FPGAs that support ECC mode RAMs. This feature may be selectively applied to individual RAMs or globally across the design.



Distributed TMR and Global TMR triple sequential elements, combinatorial logic, and majority voter.

Error Detection

Some applications do not require error correction or mitigation inside the FPGA; they require error detection and then take corrective action outside of the FPGA. With Precision Hi-Rel, designers have the ability to detect errors on selected instances and collate them into a single-bit error signal, which can be read from the FPGA for corrective action. In case of ECC RAMs, double-bit error detection is available as well.

DO-254 Design Assurance

The Precision Hi-Rel product incorporates the following mil-aero and safety-critical features:

- Repeatability of results for both register transfer level (RTL) synthesis and physical synthesis.
- Assured synthesis mode for formally verifiable synthesis.
- Formal equivalence checking with the Siemens EDA FormalPro™ product.
- Requirements tracing with the Siemens EDA ReqTracer™ technology.

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