

# Siemens Digital Industries Software Advanced FPGA Synthesis Technologies

#### **Benefits**

- FPGA vendor independent synthesis
- Excellent quality of results
- Industry leading language support for Verilog, VHDL, SystemVerilog
- Award-winning design analysis
- Precise-IP™ FPGA vendor independent IP platform
- Unique integration between synthesis and Siemens FPGA tools

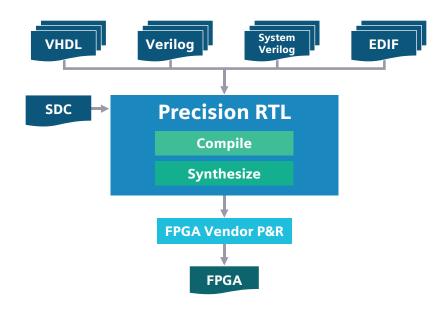
Siemens entry-level FPGA synthesis offering excellent quality of results, award-winning analysis tools, and FPGA vendor-independent solution. Includes industry-leading Verilog, VHDL, System-Verilog and mixed-language support.

## **Industry-leading FPGA synthesis**

With a rich feature set that includes advanced optimizations, award-winning analysis, and industry-leading language support, Precision RTL enables vendor-independent design, accelerates time to market, eliminates design defects, and delivers superior quality of results.

## FPGA vendor independent synthesis

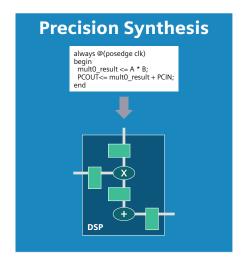
Precision RTL FPGA vendor independent synthesis allows you to target across multiple FPGA vendors such as Intel (Altera), Lattice, Microchip (Microsemi), QuickLogic or Xilinx. Designers may use the same HDL and constraint inputs for any vendor/device. This enables you to choose the best device for your design based on performance, area, power and price.



# **Precision RTL**

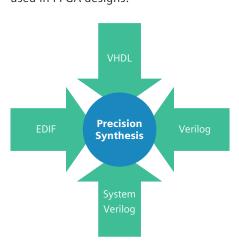
### **Excellent quality of results**

Meet performance goals quickly with Precision RTL's advanced technology-independent as well as technology-specific timing-driven optimizations. Area and timing are further optimized by using FPGA vendor-specific inference of specialized FPGA resources such as DSPs, RAMs, shift registers & carry chains.



### Industry leading language support

Precision RTL is an industry-leader offering the broadest coverage of HDL language support among the FPGA synthesis tools. Designers may use any combination of Verilog, VHDL, SystemVerilog, and EDIF languages. It supports timing constraints in the SDC (Synopsys Design Constraint) format used in FPGA designs.



#### Award-winning design analysis

Precision RTL's award-winning design tools include RTL and gate-level technology schematics and reports to understand the post-synthesis results. It also allows designers to cross-probe from generated reports, to the post-synthesis technology schematic, to the generic RTL schematic, up to the relevant HDL code to understand all issues in their appropriate contexts. With Precision's unique interactive static-timing engine it is very easy to perform what-if timing analysis for constraint refinement before running FPGA vendor place-and-route.

# Precise-IP™: FPGA vendor independent IP Platform

As part of a complete FPGA vendor independent methodology, Precision RTL features Precise-IP™, a platform allowing designers to generate a wide selection of pre-verified IP for superior quality of results (QoR) across diverse FPGA families. In addition, Precision has partnered with leading IP vendors to offer a wide selection of cores validated for use with Precision Synthesis.

# Integration with Siemens FPGA design tools

Precision RTL offers extensive integration with other Siemens FPGA design solutions, from design creation to PCB implementation:

- Catapult HLS for C++/SystemC to RTL synthesis
- HDL Designer™ for an integrated environment from design creation to implementation
- FormalPro™ for logic equivalence checking
- I/O Optimizer for FPGA and PCB co-design

#### Part of the Precision Synthesis family

The Precision Synthesis family includes products to encompass every type of user. Precision RTL, Siemens' entry-level FPGA synthesis solution, offers an excellent quality of results, industryleading language support, and an FPGA vendor-independent solution. Precision RTL Plus, Siemens' flagship FPGA synthesis and validation solution, offers best-in-class quality of results, breakthrough advantages for commercial and mil-aero applications. Precision Hi-Rel, Siemens' groundbreaking FPGA synthesis solution, offers a comprehensive & user-friendly environment for mitigation of SEUs/SETs in safety-critical & high-reliability applications.

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