The Questa Verification Solution

Benefits

Industry-Leading Solutions
- Portable stimulus and coverage closure
- Integrated verification management and analysis
- High performance/capacity unified debug
- Power-aware verification

Best-in-Class Technology
- High-performance multi-language simulator
- Formal-based apps and formal verification
- HW/SW co-verification
- UVM methodology

Enterprise Verification Platform
- Unified verification from simulation to emulation
- Simulation acceleration with Veloce TBX for up to 1000X performance gain
- Common coverage database and flows
- Unified Verification IP for acceleration and reuse

The Questa® Verification Solution from Siemens EDA, a part of Siemens Digital Industries Software, continues to evolve in response to the growing complexity of SoC designs. Besides the sheer size of designs, the inclusion of multiple embedded processors and advanced interconnect systems, increasing software content and the configurability required by multi-platform based designs require a functional verification solution that unifies a broad arsenal of verification solutions. The key to verification success is to decompose the problem and use the best solution for each aspect of the system. This places tremendous importance on the verification plan and the ability to collect metrics throughout the process and across all verification tasks to track progress against the plan, allocate and manage resources efficiently, and identify trends as the project progresses against schedule.

Software has become a major component of SoC system functionality, creating new requirements for block-to-system verification reuse and the need for system verification and debug. While software testing of SoC integration and basic functionality as well as the verification of low level driver software can be accomplished in simulation, long, complex sequences that exercise system functionality demand acceleration with full debug visibility. To avoid wasting cycles at the system level, it is critical to identify bugs as early as possible in the process. Questa lets you apply CDC verification, formal verification, mixed-signal verification, portable stimulus, and other powerful technologies to maximize the effectiveness of your verification at the block- and subsystem-level so your system-level verification can focus on system-level functionality, including software, without having to worry about lower-level bugs taking away from your productivity. No one wants to compromise product quality. However, time-to-market pressures dominate SoC projects. To deliver quality within schedule requires improving the time to achieve coverage and quality goals and improving debug productivity.

The solution is composed of several technologies, each powerful on its own. Applied together, along with a comprehensive database and best-in-class verification management tools, these technologies deliver a powerful answer to the spectrum of verification problems.

Unified Simulation is built on a best-in-class simulator. The Questa Advanced Simulator achieves industry-leading performance and capacity through very aggressive, global compile and simulation optimization algorithms for SystemVerilog and VHDL. Questa also supports very fast turnaround time flows and effective library management while maintaining high performance with unique capabilities to pre-optimize

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and reuse, enabling dramatic regression throughput improvements of up to 3X when running a large suite of tests. The Questa Visualizer debug environment provides high performance, high-capacity debugging for both Questa and Veloce, enabling the use of the same debug environment from simulation to emulation and other engines.

Portable Stimulus and Intelligent Testbench Automation.

Questa inFact automatically generates verification stimulus and can be applied at the block, subsystem and SoC levels. The technology avoids redundancy and can achieve target coverage more than 10X faster than is possible with constrained random testing. The technology can be applied to shorten time to coverage or to achieve more comprehensive verification by enabling more tests to run in the same amount of time.
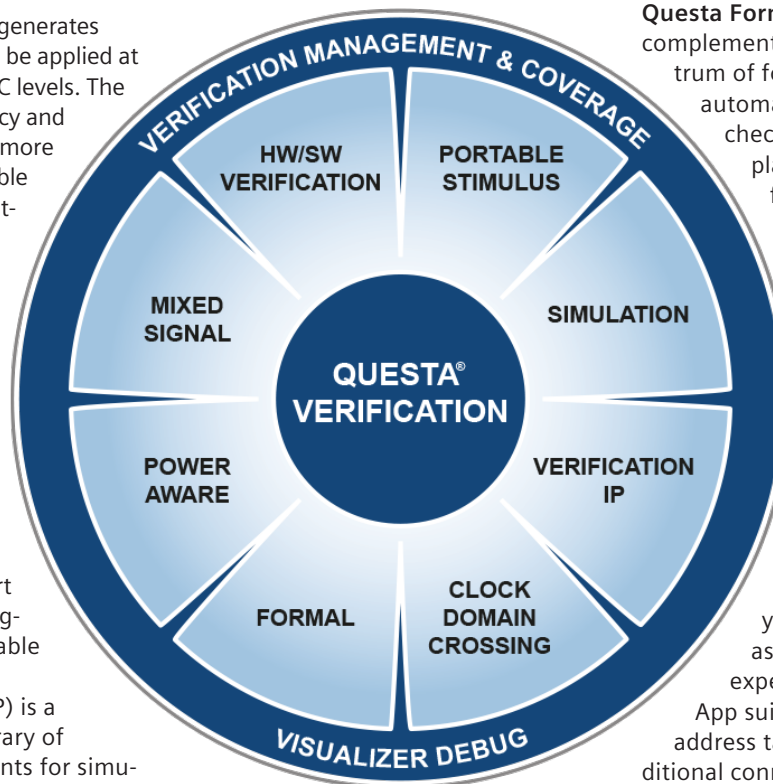
Verification IP is designed to simplify the verification of standard protocol interfaces that are complex and would take significant effort otherwise. It is highly configurable and consists of reusable testbench building blocks. Questa Verification IP (QVIP) is a performance-optimized library of standard SV UVM components for simulation with support for Arm® AMBA®, Ethernet, MIPI®, PCIe® and USB and many other protocols including some of the leading edge protocols like PCIe Gen 5. Using QVIP frees up engineers to focus on design-specific verification and enables tests to be reused in acceleration with Veloce. QVIP includes advanced transaction-level debug, comprehensive protocol assertions, functional coverage, test plans and test sequences that together can be used to validate protocol compliance and accelerate time-to-RTL-signoff.

The Questa Memory Library comprises an extensive range of fast and accurate DRAM and Flash memory models. These can be dropped into any testbench to verify any memory subsystem. For speed, we provide backdoor access and on-the-fly reconfiguration. For correctness and completeness, we provide extensive assertions and coverage. For debugging, we provide powerful transaction-to-pins debug capabilities.

Questa CDC and RDC Solutions identify errors that have to do with clock and reset domain crossings – signals (or groups of signals) that are generated in one domain and consumed in another. It does so with structural analysis and recognition of clock or reset domains, synchronizers, and low power structures (via UPF). The technology checks all potential failure modes and presents to the user familiar schematic and waveform displays. Additionally, in concert with simulation this technology can

inject metastability into functional simulation for reconvergence verification and waiver validation. Finally, Signoff CDC analysis identifies clock domain crossing issues in the final netlist of a design that weren't present in the source RTL that may have been generated by the implementation process, and does so efficiently by preserving constraints and setup from the original RTL CDC environment.

Questa Formal Verification solutions complement simulation with a full spectrum of formal tools ranging from automated apps to direct model checking. At the core of the platform is a set of high performance formal analysis engines that offer exhaustive verification early in the design cycle with custom coded SVA/PSL/OVL assertions. Building on this foundation, the Questa Formal Apps boost verification efficiency and design quality by exhaustively addressing verification tasks that are difficult to complete with traditional methods, yet do not require formal or assertion-based verification experience. The Questa Formal App suite includes applications to address tasks such as: static and conditional connectivity checking, secure path integrity checking, unreachable code identification, X-state propagation, state-space analysis, and register verification. Additionally, the Questa Sequential Logic Equivalence Checking (SLEC) App uses formal methods to perform exhaustive comparisons between inputs to reveal any behavioral discrepancies that could arise in clock gating, ECO integration, re-pipelining, or fault mitigation logic. For interactive formal model checking, users write properties for assertions (tests), assumes (constraints), and coverage, then run

Questa PropCheck to reveal any discrepancies between the specification and DUT. Model checking can also address issues of interface protocols, functional coverage, control logic, data integrity, and post-silicon debug, which, together, provide the most exhaustive possible analysis of a design. Formal-optimized Verification IP is available for popular standard protocols.

Questa Low Power Verification enables early (RTL) verification of active power management applied to a complex design, to ensure that the power management architecture and behavior are correct and that the design will operate correctly under active power management. Questa PowerAware simplifies the verification process through a comprehensive suite of static checkers for checking the consistency of the power management architecture and dynamic checks for automated error detection. Questa PowerAware also provides visualization of power management architecture and behavior, coverage data collection, and test plan generation for power states and state transitions. Based on the latest industry-standard IEEE 1801-2015 UPF for specification of active power management, Questa PowerAware integrates well with other UPF-based tools to support multi-tool and multi-vendor low power design and verification flows.

Questa ADMSTM verifies complex analog/mixed-signal designs. The technology integrates four high performance engines: Eldo® for general purpose analog, ADiTTM for fast transistor-level, Eldo RF for modular steady state and Questa Sim for digital. Its combination of languages and algorithms allows for both top-down design and bottom-up

verification supporting multiple levels of abstraction and performance from Spice netlists to Real Number Models.

Questa HW/SW Verification provides processor-based system-level verification, using software tests to verify RTL and hardware/software integration. The technology comes with a host of advantages such as ensuring chip power management, loading and booting operating systems, and running software applications. It accelerates simulation, enables instant replay, and offers virtual emulation — all of which serve to trim debugging time.

Questa Verification Management and Coverage manages the data complexity, guides the process and provides automation across all verification engines to improve verification productivity. It offers analysis and optimization features built upon the Unified Coverage Interoperability Standard database (UCISDB), with results and trend analysis, test plan tracking and run management. Questa Verification Management efficiently ties all verification-related tasks together and gives all parties — system architects, software engineers, designers and verification specialists — real-time visibility into the project. This visibility helps to hit market windows on schedule, manage risk and improve throughput and debug turnaround times.

Questa Visualizer is a context-aware debug platform that supports a complete logic verification flow, including simulation, emulation, and prototyping as well as design, testbench, low-power, and assertion analysis. Visualizer provides a high performance/high capacity debugger that scales from simulation to emulation. Multiple automated features quickly find RTL, gate-level, and protocol

bugs. Low-power and UPF debug is fully integrated and overlaid with RTL views. Visualizer is SystemVerilog class-based and UVM-aware to speed up overall debug time, even on today's most complex SoCs and FPGAs.
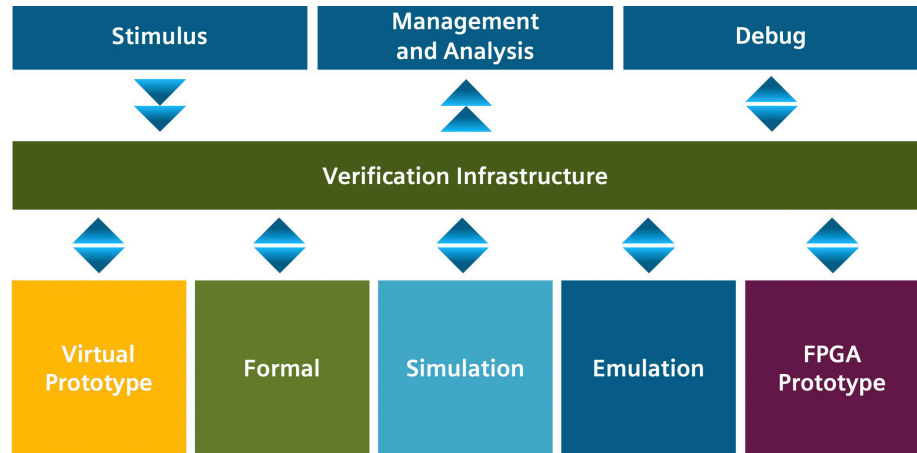
Siemens EDA Verification Expertise provides ample resources to help you get started adopting advanced verification techniques.

The Verification Academy is organized into a collection of free online courses and resources, focusing on key aspects of advanced functional verification designed to mature an organization's verification process. Course topics include Assertion-Based Verification, Clock-Domain Crossing Verification, Formal Assertion-Based Verification, Formal Coverage, Metrics in SoC Verification, Portable Stimulus, Power Aware Simulation, UVM Debug, and many more. Each course consists of multiple sessions allowing the viewer to pick and choose topics of interest as well as revisit topics for future reference.

The Verification Academy is the most complete UVM online resource collection. You'll find everything you need to get up to speed on UVM, whether it's downloading the kit(s) or participating in online or in-person training. The UVM courses provide a great overview of methodology concepts, introductory to advanced, with videos that walk through useful code examples. The UVM Online Methodology Cookbook is an online textbook to show you in more detail how to use the various features of the methodologies to create reusable verification components and environments.

Consulting and Training. Siemens EDA Consulting Verification Services offers solution-driven consultants who will dramatically reduce your verification process times while improving quality. Unlike other EDA consulting services or third party consultants, Siemens EDA Consulting's highly experienced Verification Services team offers customized solutions and proven, structured processes to ensure projects are delivered on time and to specification, and with greater probability of first-pass success. Siemens EDA Education Services offers a full range of learning solutions developed specifically for electronics designers and engineers engaged in advanced verification. Users can choose the type of training that best suits their needs and schedule. These choices include unique Live Online Training, training and seminars given in Siemens EDA training centers around the world, and on-site training and mentoring specifically designed for your company.

The Enterprise Verification Platform. Built upon several powerful technologies, the Enterprise Verification Platform transforms verification, dramatically increasing productivity and more efficiently managing resources, enabling users to select the best application or tool for the job and combine results from all the engines to dynamically track the progress of the entire verification program.

| Stimulus | Management and Analysis | Debug |

Verification Infrastructure

| Virtual Prototype | Formal | Simulation | Emulation | FPGA Prototype |

The Siemens EDA Enterprise Verification Platform (EVP) delivers high performance verification from prototype to silicon.